U.S. Patent Application No. 10/722,593 Docket No. 4590-242

REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1, 2 and 4-20 remain pending in the application.

Claims 1, 2 and 4-20 are rejected under 35 U.S.C. 112, as being indefinite. In response, the claims have been amended and the rejection should be withdrawn.

Claims 10-11 and 13-16 are rejected under 35 U.S.C. 102 that form the basis for the rejections. In response, claim 10 has been amended and is believed to be patentable over Pertersson et al (US 5,140,284) for the reasons discussed below.

The inventiveness of the present patent application is notably:

1) varying the length of the cycle of the command N / N+1 / N+2 /... of the divider Na and making this length variable according to the rank Nb of the output divider.

2) to give a method of choice of the values of Nb and the ratio Fref / Δ F so that the different lengths of cycle correspond to multiple integers of the reference frequency Fref of the phase comparator of the loop.

In Pertersson et al, in column 3, line 45-52, the circuit 27 allows the value of dividers 21, 25 and 26 according to a given output frequency Fout to be adjusted.

This modification of the values of 21, 25 and 26 by 27 corresponds to the phase lock-in process of phase-locked loop as it is confirmed in column 3, line 52-64.

In the present patent application, there is a triple variation attached to the divider of loop Na.

The Figure 6 of present application shows clearly that the value Na may vary from 15 to 21: it is the first variation of Na that can be qualified as static and corresponding to the phase lock-in process of phase loop (as in Pertersson et al).

There is then a second variation of Na, that one dynamics, because it is processed at the rate of the frequency of comparison of loop phase, that is 144 MHz. It means that all 6.94 ns, the value of Na is modified by 0,1 or 2 units thanks to the thread of signal control named N / N+1 / N+2. This dynamic variation corresponds to the fractional functioning of the Synthesizer.

The fractional step Na of the loop divider thus varies from 0 to 2 units at the rate of the frequency 144 MHz (reference frequency of the comparator of phase).

This variation is cyclic (it takes place according to a periodic sequence), that is why in the present patent application, it is question of the cycle of evolution of Na.

According to the devices of the previous art, the length of this cycle is constant.

In the present patent application, the idea of the intention consists, notably, in making, more, the length of this cycle vary, what constitutes the 3rd variation concerned to the divisor Na. The length of this cycle is chosen by a table according to the value of the divisor Nb (see for example in Figure 6). On this example each of the lengths of cycle expressed in number of period of Fref=144 MHz is the product of prime numbers amongst them.

The divider Nb may be adjusted and can take the values 9, 10, 12 or 15 for the example of the Figure 6.

In the opinion of the Applicant, the technical teaching of Pertersson et al does not disclose nor suggests the characteristics claimed in the amended claim 1.

The technique of the fractional Synthesis was introduced for the first time into the US Patent N 3,928,813 of A. KINGSFORD-SMITH on December 23, 1975 and entitled "Device for Synthesizing Frequencies which are rational multiples of a fundamental Frequency". Since this date, numerous publications and patents were allowed on this subject.

On the other hand, the technical problem to be resolved in the present patent application (see page 2, line 16-31 of the present patent application) was already known by Pertersson et al (see the specification of Pertersson et al) :

1) The difficulty realizing the VCO is mentioned in column 2, line 1-4 of Pertersson et al

2) The necessity of fast switching time is described in column 2, line 22-25

3) The need of a low phase noise and low spurious is described in column 2, line 22-25.

In 1992, date of the Publication of the patent of Pertersson et al, the problem previously mentioned was known. Since this time, no document has disclosed or suggested the characteristics claimed in the amended claim.

Applicant submits that the present invention is new and inventive in view of the prior art. Accordingly, the anticipation rejection should be withdrawn.

Moreover, method according to the present patent application allows a faster switching

time (because greater loop bandwith described in the present patent application) and also lower phase noise and lower spurious lines (because division ranks of the loop divider in the present patent application are lower than those of Pertersson et al).

Claims 1-2, 4-9, 12-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Petersson et al (US 5,140,284) in view of Dekker (US 6,239,660). In response, claim 1 has been amended and is believed to be patentable over Petersson in view of Dekker.

Claims 1-2 and 4-9 are apparatus claims corresponding to the method claims discussed above and should be patentable for the reasons discussed above. Accordingly, this rejection should be withdrawn.

Early issuance of a Notice of Allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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